



IN THE CLAIMS

Please amend claims 2, 11 and 20, and add claims 28-30 as follows:

1 1.(Original) In a communications system including a receiver
2 device for receiving symbols communicated via a communications
3 channel and encoded according to a Complementary Code Key (CCK)
4 chip encoding scheme, a system for decoding received CCK encoded
5 symbols (chips), said system comprising:
6 a decision feedback equalizer (DFE) structure for receiving
7 and equalizing CCK-encoded symbols communicated over a
8 communications channel, and providing an output comprising an
9 estimation of said received symbols, said DFE structure including a
10 forward equalizer path and a feedback equalizer path including a
11 feedback filter;
12 a CCK decoder means embedded in said feedback path and
13 operating in conjunction with a feedback filter therein for
14 decoding said chips, said decoding of CCK chips being based on
15 intermediate DFE outputs including those chips corresponding to
16 past decoded CCK symbols,
17 wherein decisions on a symbol chip at a particular time are
18 not made until an entire CCK codeword that the chip belongs to is

19 decoded, thereby reducing errors propagated when decoding said
20 symbols.

1 2. (Currently Amended) The system according to Claim 1,
2 wherein the decoding and equalization are performed on a block of
3 | eight 8 chips of said intermediate DFE outputs (\tilde{c}_{k+j}) for CCK modes.

1 3. (Original) The system according to Claim 2, wherein
2 estimated DFE equalizer outputs \tilde{c}_{k+j} for CCK mode symbols is
3 governed according to the equation:

$$4 \quad \tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^j b_i c_{k+j-i}, \text{ where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i}$$

5 $j=0, \dots, 7$ and represents the intermediate DFE equalizer outputs
6 that include, in the feedback filter, only those chips
7 corresponding to past decoded CCK symbols, f_i are forward equalizer
8 taps, b_i are feedback equalizer taps, r_k represents a received input
9 stream at a specified rate, L_f represents a length of the forward
10 filter, d_f represents a delay through the forward filter, L_b
11 represents a length of the feedback filter, and \hat{c}_k represents a
12 slicer output which is an estimate of the true transmitted chip c_k ,

13 and the $\sum_{i=1}^j b_i c_{k+j-i}$ component represents the chips comprising the
14 present transmitted symbol.

1 4.(Original) The system according to Claim 3, wherein the CCK
2 decoder includes means for choosing from a set of possible CCK
3 codewords, a codeword $\underline{c} = [c_0, c_1, \dots, c_7]$ that minimizes a metric
4 comprising:

5
6
$$\sum_{j=0}^7 \left| s_{k+j} + \sum_{i=1}^j b_i c_{j-i} - c_j \right|^2 .$$

1 5.(Original) The system according to Claim 4, wherein the
2 codeword \underline{c} is represented in terms of variables α_i and ϕ_1 according
3 to

4
$$\underline{c} = e^{j\phi_1} \underline{d} \text{ where } \underline{d} = [e^{j\alpha_1}, e^{j\alpha_2}, e^{j\alpha_3}, -e^{j(\alpha_2+\alpha_3-\alpha_1)}, e^{j(2\alpha_1-\alpha_2-\alpha_3)}, e^{j(\alpha_1-\alpha_3)}, -e^{j(\alpha_1-\alpha_2)}, 1]$$

5 and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$,
6 whereby \underline{d} belongs to a set of 64 possible state vectors, and \underline{c} may
7 have 256 possible values.

6.(Original) The system according to Claim 5, wherein the CCK decoder includes trellis decoding means for generating a trellis structure having a plurality of trellis paths representing possible states of said codeword \underline{c} , wherein a state in the trellis structure is represented by the vector $[\alpha_1, \alpha_2, \alpha_3]$.

7.(Original) The system according to Claim 6, wherein said metric to be minimized is governed according to:

$$\sum_{j=0}^7 |\chi_j|^2 + 2\text{Re} \left[e^{j\phi} \sum_{j=0}^7 s_{k+j}^* \chi_j \right] \text{ where } \chi_j = \sum_{i=0}^j b_i d_{j-i}.$$

8.(Original) The system according to Claim 7, wherein the metric to be minimized is governed according to

$$\sum_{j=0}^7 m_1(j) + 2\text{Re} \left[e^{j\phi} \sum_{j=0}^7 m_2(j) \right] \text{ where } m_1(j) = |\chi_j|^2 \text{ and is a real-valued}$$

quantity, and $m_2(j) = s_{k+j}^* \chi_j$ and is a complex-valued quantity, said trellis decoder structure including means for processing a block of eight (8) intermediate output symbols s_{k+j} , $j = 0, 1, \dots, 7$, including means for calculating, at each time, j , for each branch in a trellis path, said $m_1(j)$ and $m_2(j)$ quantities; and, means for adding $m_1(j)$ and $m_2(j)$ quantities to the corresponding quantities of

10 the state from which the trellis branch originated, whereby the
11 eight intermediate outputs s_{k+j} , $j = 0, 1, \dots, 7$, are processed by
12 the trellis to determine the transmitted codeword at time k .

1 9. (Original) The system according to Claim 8, wherein said
2 calculating means includes calculating, for each codeword state,
3 the $\sum_{j=0}^7 m_1(j) + 2\text{Re}\left[e^{j\phi_1} \sum_{j=0}^7 m_2(j)\right]$ metric for each of four ϕ_1 values
4 $[0, \pi/2, \pi, 3\pi/2]$, said means further choosing a state vector $[\alpha_1, \alpha_2, \alpha_3]$
5 and ϕ_1 that results in the minimum metric and calculating the
6 transmitted codeword \underline{c} accordingly therefrom, wherein a
7 dimensionality of said trellis decoding means is reduced from 256
8 to 64.

1 10. (Currently Amended) A method for decoding symbols encoded
2 according to a Complementary Code Key (CCK) chip encoding scheme,
3 said method comprising the steps of:

4 a) providing a decision feedback equalizer (DFE) structure for
5 receiving and equalizing CCK-encoded symbols (chips) communicated
6 over a communications channel, said DFE structure further
7 estimating said received symbols for DFE output, said DFE structure
8 including a forward equalizer path and a feedback equalizer path

9 including a feedback filter;

10 b) embedding a CCK decoder means in said feedback path for
11 decoding said chips in conjunction with filter taps ~~of~~ determined
12 for said feedback filter; and,

13 c) decoding of said CCK chips based on intermediate DFE
14 outputs including those chips corresponding to past decoded CCK
15 symbols,

16 wherein decisions on a symbol chip at a particular time are
17 not made until an entire CCK codeword that the chip belongs to is
18 decoded, thereby reducing errors propagated when decoding said
19 symbols.

1 11.(Currently Amended) The method according to Claim 10,
2 wherein the decoding and equalization steps are performed on a
3 block of eight 8 chips of said intermediate DFE outputs (\tilde{c}_{k+j}) for
4 CCK modes.

1 12.(Original) The method according to Claim 11, wherein said
2 estimating step includes calculating estimated DFE equalizer
3 outputs \tilde{c}_{k+j} for CCK mode symbols according to:

$$\tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^j b_i c_{k+j-i}, \text{ where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i} \quad j=0, \dots, 7$$

and represents the intermediate DFE equalizer outputs that include, in the feedback filter, only those chips corresponding to past decoded CCK symbols, f_i are forward equalizer taps, b_i are feedback equalizer taps, r_k represents a received input stream at a specified rate, L_f represents a length of the forward filter, d_f represents a delay through the forward filter, L_b represents a length of the feedback filter, and \hat{c}_k represents a slicer output which is an estimate of the true transmitted chip c_k , and the $\sum_{i=1}^j b_i c_{k+j-i}$ component represents the chips comprising the present transmitted symbol.

13.(Original) The method according to Claim 12, further including the step of: choosing from a set of possible CCK codewords, a codeword $\underline{c} = [c_0, c_1, \dots, c_7]$ that minimizes a metric comprising:

$$\sum_{j=0}^7 \left| s_{k+j} + \sum_{i=1}^j b_i c_{j-i} - c_j \right|^2.$$

14.(Original) The method according to Claim 13, wherein the

2 codeword \underline{c} is represented in terms of variables α_i and ϕ_i according
3 to $\underline{c} = e^{j\phi_1} \underline{d}$ where $\underline{d} = [e^{j\alpha_1}, e^{j\alpha_2}, e^{j\alpha_3}, -e^{j(\alpha_2+\alpha_3-\alpha_1)}, e^{j(2\alpha_1-\alpha_2-\alpha_3)}, e^{j(\alpha_1-\alpha_3)}, -e^{j(\alpha_1-\alpha_2)}, 1]$
4 and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$,
5 whereby \underline{d} belongs to a set of 64 possible vectors, and \underline{c} may have
6 256 possible values.

1 15.(Original) The method according to Claim 14, wherein said
2 decoding step c) further includes the step of generating a trellis
3 structure having a plurality of trellis paths representing possible
4 states of said codeword \underline{c} , wherein a state in the trellis structure
5 is represented by the vector $[\alpha_1, \alpha_2, \alpha_3]$.

1 16.(Original) The method according to Claim 15, wherein said
2 metric to be minimized is governed according to:

$$3 \quad \sum_{j=0}^7 |\chi_j|^2 + 2\text{Re} \left[e^{j\phi_1} \sum_{j=0}^7 s_{k+j}^* \chi_j \right] \text{ where } \chi_j = \sum_{i=0}^j b_i d_{j-i} \dots$$

1 17.(Original) The method according to Claim 16, wherein the
2 metric to be minimized is governed according to

$$3 \quad \sum_{j=0}^7 m_1(j) + 2\text{Re} \left[e^{j\phi_1} \sum_{j=0}^7 m_2(j) \right] \text{ where } m_1(j) = |\chi_j|^2 \text{ and is a real-valued}$$

4 quantity, and $m_2(j) = s_{k+j}^* \chi_j$ and is a complex-valued quantity, said

5 trellis generating step further including the steps of:

6 processing a block of eight (8) intermediate output symbols

7 s_{k+j} , $j = 0, 1, \dots, 7$, including means for calculating, at each time,

8 j , for each branch in a trellis path, said $m_1(j)$ and $m_2(j)$

9 quantities; and,

10 adding said $m_1(j)$ and $m_2(j)$ quantities to the corresponding

11 quantities of the state from which the trellis branch originated,

12 whereby the eight intermediate outputs s_{k+j} , $j = 0, 1, \dots, 7$, are

13 processed by the trellis to determine the transmitted codeword at

14 time k .

1 18.(Original) The method according to Claim 17, wherein the

2 calculating step further includes the steps of:

3 calculating, for each codeword state, the

4 $\sum_{j=0}^7 m_1(j) + 2\text{Re}\left[e^{j\phi_1} \sum_{j=0}^7 m_2(j)\right]$ metric for each of four ϕ_1 values $[0, \pi/2, \pi, 3\pi/2]$;

5 and,

6 choosing a state vector $[\alpha_1, \alpha_2, \alpha_3]$ and ϕ_1 that results in the

7 minimum metric and calculating the transmitted codeword \underline{c}

8 accordingly therefrom, wherein a dimensionality of said trellis

9 structure is reduced from 256 to 64.

1 19.(Original) A receiver device for receiving symbols
2 communicated via a communications channel, said symbols encoded
3 according to a Complementary Code Key (CCK) chip encoding scheme,
4 said receiver device comprising:

5 a decision feedback equalizer (DFE) structure for receiving
6 and equalizing CCK-encoded symbols (chips) communicated over a
7 communications channel, and providing an output comprising an
8 estimation of said received symbols, said DFE structure including a
9 forward equalizer path and a feedback equalizer path including a
10 feedback filter;

11 a CCK decoder means embedded in said feedback path and
12 operating in conjunction with a feedback filter therein for
13 decoding said chips, said decoding of CCK chips being based on
14 intermediate DFE outputs including those chips corresponding to
15 past decoded CCK symbols,

16 wherein decisions on a symbol chip at a particular time are
17 not made until an entire CCK codeword that the chip belongs to is
18 decoded, thereby reducing errors propagated when decoding said
19 symbols.

20.(Currently Amended) The receiver device according to Claim 19, wherein the decoding and equalization are performed on a block of eight 8 chips of said intermediate DFE outputs (\tilde{c}_{k+j}) for CCK modes.

21.(Original) The receiver device according to Claim 20, wherein estimated DFE equalizer outputs \tilde{c}_{k+j} for CCK mode symbols is governed according to the equation:

$$\tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^j b_i c_{k+j-i}, \text{ where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i} \quad j=0, \dots, 7$$

and represents the intermediate DFE equalizer outputs that include, in the feedback filter, only those chips corresponding to past decoded CCK symbols, f_i are forward equalizer taps, b_i are feedback equalizer taps, r_k represents a received input stream at a specified rate, L_f represents a length of the forward filter, d_f represents a delay through the forward filter, L_b represents a length of the feedback filter, and \hat{c}_k represents a slicer output which is an estimate of the true transmitted chip c_k , and the

$\sum_{i=1}^j b_i c_{k+j-i}$ component represents the chips comprising the present transmitted symbol.

1 22.(Original) The receiver device according to Claim 21,
2 wherein the CCK decoder includes means for choosing from a set of
3 possible CCK codewords, a codeword $\underline{c} = [c_0, c_1, \dots, c_7]$ that minimizes
4 a metric comprising:

5
$$\sum_{j=0}^7 \left| s_{k+j} + \sum_{i=1}^j b_i c_{j-i} - c_j \right|^2 .$$

1 23.(Original) The receiver device according to Claim 22,
2 wherein the codeword \underline{c} is represented in terms of variables α_i and
3 ϕ_1 according to $\underline{c} = e^{j\phi_1} \underline{d}$ where \underline{d}

4
$$= [e^{j\alpha_1}, e^{j\alpha_2}, e^{j\alpha_3}, -e^{j(\alpha_2+\alpha_3-\alpha_1)}, e^{j(2\alpha_1-\alpha_2-\alpha_3)}, e^{j(\alpha_1-\alpha_3)}, -e^{j(\alpha_1-\alpha_2)}, 1]$$

5 and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$,
6 whereby \underline{d} belongs to a set of 64 possible vectors, and \underline{c} may have
7 256 possible values.

1 24.(Original) The receiver device according to Claim 23,
2 wherein the CCK decoder includes trellis decoding means for
3 generating a trellis structure having a plurality of trellis paths

4 representing possible states of said codeword \underline{c} , wherein a state in
5 the trellis structure is represented by the vector $[\alpha_1, \alpha_2, \alpha_3]$.

1 25.(Original) The receiver device according to Claim 24,
2 wherein said metric to be minimized is governed according to:

3
$$\sum_{j=0}^7 |\chi_j|^2 + 2\text{Re} \left[e^{j\phi} \sum_{j=0}^7 s_{k+j}^* \chi_j \right] \text{ where } \chi_j = \sum_{i=0}^j b_i d_{j-i} \dots$$

1 26.(Original) The receiver device according to Claim 25,
2 wherein the metric to be minimized is governed according to

3
$$\sum_{j=0}^7 m_1(j) + 2\text{Re} \left[e^{j\phi} \sum_{j=0}^7 m_2(j) \right] \text{ where } m_1(j) = |\chi_j|^2 \text{ and is a real-valued}$$

4 quantity, and $m_2(j) = s_{k+j}^* \chi_j$ and is a complex-valued quantity, said
5 trellis decoder structure including means for processing a block of
6 eight (8) intermediate output symbols s_{k+j} , $j = 0, 1, \dots, 7$,
7 including means for calculating, at each time, j , for each branch
8 in a trellis path, said $m_1(j)$ and $m_2(j)$ quantities; and, means for
9 adding $m_1(j)$ and $m_2(j)$ quantities to the corresponding quantities of
10 the state from which the trellis branch originated, whereby the
11 eight intermediate outputs s_{k+j} , $j = 0, 1, \dots, 7$, are processed by
12 the trellis to determine the transmitted codeword at time k .

1 27.(Original) The receiver device according to Claim 26,
2 wherein said calculating means includes calculating, for each
3 codeword state, the $\sum_{j=0}^7 m_1(j) + 2\text{Re}\left[e^{j\phi_1} \sum_{j=0}^7 m_2(j)\right]$ metric for each of four
4 ϕ_1 values $[0, \pi/2, \pi, 3\pi/2]$, said means further choosing a state vector
5 $[\alpha_1, \alpha_2, \alpha_3]$ and ϕ_1 that results in the minimum metric and
6 calculating the transmitted codeword \underline{c} accordingly therefrom,
7 wherein a dimensionality of said trellis decoding means is reduced
8 from 256 to 64.

1 28.(New) The system according to Claim 1, wherein the CCK
2 decoder includes a trellis decoder having a number of trellis
3 paths, wherein said number of trellis paths is less than all
4 possible states of said entire CCK codeword that the chip belongs
5 to.

1 29.(New) The method according to Claim 10, wherein said
2 decoding step c) further includes the step of generating a trellis
3 structure having a number of trellis paths, wherein said number of
4 trellis paths is less than all possible states of said entire CCK
5 codeword that the chip belongs to.

1 30.(New) The receiver device according to Claim 19, wherein
2 the CCK decoder includes a trellis decoder having a number of
3 trellis paths, wherein said number of trellis paths is less than
4 all possible states of said entire CCK codeword that the chip
5 belongs to.